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ABSTRACT

A process for the fabrication of an integrated circuit which provides a FET device having reduced GIDL current is described. A semiconductor substrate is provided wherein active regions are separated by an isolation region, and a gate oxide layer is form on the active regions. Gate electrodes are formed upon the gate oxide layer in the active regions. An angled, high dose, ion implant is performed to selectively dope the gate oxide layer beneath an edge of each gate electrode in a gate-drain overlap region, and the fabrication of the integrated circuit is completed.